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# Saturation Throughput and Delay Aware Asynchronous Noc Using Fuzzy Logic

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Abstract-Due to scaling in recent trends in modern semiconductor industries, critical instance such as voltage spikes, temperature, interlink between IC circuits has been improvised under the design. The saturation throughput and average message delay are used as performance metrics to evaluate the throughput. We introduced the fuzzy logic based asynchronous NoC to attain the high throughput and diminish the delay between the inter logic circuits aim to select the less congested paths to produce load balance in the network especially under realistic traffic loads. Our Fuzzy logic based routing algorithm is an adaptive, low cost, and scalable. It outperforms against different adaptive routing algorithms in the average delay and saturation throughput for various traffic patterns. STDR can achieve up to 12%–32% average message delay lower than that of other routing algorithms. Moreover, the proposed scheme yields improvements in saturation throughput by up to 11%–82% compared with other adaptive routing algorithms.

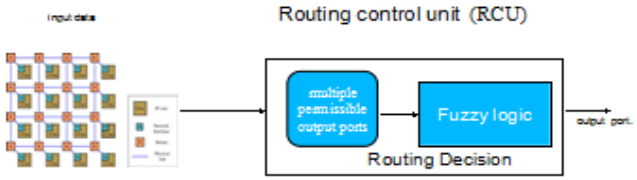
Index Terms—Asynchronous design, congestion, network on chip (NoC), process variation (PV), routing algorithms.

## I. INTRODUCTION

International Technology Roadmap for Semiconductors presents the process variation (PV) parameters as a critical challenge for IC manufacture. Systematic and random variations are two sources for PV. With technology scaling down, random variation becomes significantly larger than systematic variation. Random variation appears in logic gates and interconnects. The impact of random PV emerged on low and high levels of designs.One of the key factors of designing network on chip (NoC)is the routing algorithm. An efficient routing algorithm is required to achieve high performance. Hence, ignoring the impact of PV during the design of any routing algorithm results in unexpected average message delay and saturation throughput. Average message delay and saturation throughput are used as two metrics to evaluate the performance of a routing algorithm.

The saturation throughput occurs when no additional messages can be injected successfully to the network . Prior to the saturation throughput, the averagemessage delay slightly increases with the injection load..However, the average message delay increases exponentially beyond the network saturation ,.As a hardware solution, a new router design is proposed to mitigate PV impact. In variation-adaptive variable-cycle router configures its cycle latency adaptively corresponding to the spatial PV to increase the network frequency in the synchronous network. Adaptive routing algorithm for multicore NoC architectures is presented in to reduce saturation bandwidth degradation caused by PVs.In source routing algorithm is introduced to enhance the speed of the communication in an NoC based on the PV.To the best of our knowledge, the work presented in this paper is the first work to investigate the impact of PV on different routing algorithms. Moreover, an adaptive routing algorithm that is aware of the PV and congestion for asynchronous NoC designs is introduced..

**BLOCK DIAGRAM:**
**AYSNCHRONOUS DESIGN WITH THE RCU BLOCK:**




In this paper, a novel adaptive routing algorithm is proposed for asynchronous NoC designs to reduce the effect of PV. The presented algorithm is applicable with any source of PV.The technique is insensitive to the source of the variation.The novel routing algorithm uses the PV and congestion information as metrics to select the suitable output port (OP). In addition, the realistic values of average message delay and saturation throughput under high PV for different routing algorithms are compared with that of the nominal values (without PV).This paper is organized as follows. In Section II,Background of PV in asynchronous NoC.The STDR routing algorithm is described in Section III. In Section IV Fuzzy logic and in section V simulation results are provided. Some conclusions are demonstrated in Section VI.

## II. BACK GROUND

### 2.1.1 Process Variation :

Technology scaling increases the threshold-voltage (Vth) variation of MOS transistors composed of die-to-die (D2D) and within-die (WID) variations, of which the WID variation is divided into systematic and random variations.The WID variation because it affects the characteristics of individual cores within a die, which turns out to be core-to-core (C2C) variation. Systematic variation results mainly from lens aberration and has a spatial correlation . Therefore, neighboring transistors have similar characteristics. In contrast, random variation results mainly from random do pant fluctuation (RDF) and line-edge roughness (LER): random variations show no spatial correlation. For that reason, individual transistors have different characteristics from those of neighbouring transistors.

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**2.1.2 Process Variation in NoC :**

Process variation in an NoC shows up as variation of operating frequencies of individual cores. Considering synchronous designs for entire NoC processor cores in situations where operating frequencies vary, each core in the NoC must synchronize with the slowest core. There- fore, the throughput of the entire NoC processor degrades with increasing impact of the process variation. Global- asynchronous local-synchronous (GALS) designs, in which the fabric with individual cores and network elements operate at their own maximum frequencies, are widely adopted in NoC design. The network portion composed of routers, wires, and buffers is designed frequently at a single frequency and in a single voltage domain .because the design of the network portion in an NoC is too complicated and overly costly. This issue is extremely important in a large NoC fabricated using scaled process technology. A processor core and a router communicate asynchronously with each other at a different frequency. An operating frequency in a processor core is determined by each maximum operating frequency.

**2.1.3 Impact of Variation in Processor Core :**

This section presents a description of the impact of the process variation to the processor core. Assuming a 20 FO4 inverter chain delay as a single pipeline stage in the processor core, we conducted Monte Carlo simulations in a 65-nm process technology using a SPICE circuit simulator. The systematic variation in a threshold voltage (*V*th) arises as C2C variation. In this simulation, the standard deviation of the systematic variation, $\sigma_{system}$, is calculated with, as 6.3% of the average *V*th. Random variation is apparent at individual transistors. Consequently, it affects all circuits in the core. We use standard deviations of random variations in NMOSes and PMOSes from actual measurement. The distribution of the operating frequencies obtained through simulations of 20 FO4 inverters. We set four frequency bins: 800 MHz, 1,100 MHz, 1,200 MHz, and 1,300 MHz. The operating frequency variation derived from the *V*th variation is apparent as a normal distribution. The standard deviation of the operating frequencies,in the 20 FO4 inverters is 145.4 MHz. Accordingly, the individual processor cores in an NoC under the *V*th variation represent mutually differing operating frequency characteristics.

**2.1.4 Impact of Variation in On-Chip Networks:**

Depicts the organization of a router with virtual channels (VCs) .Presents a Gantt chart of each pipeline stage of the router. The pipeline stages are described as follows. The next routing computation stage (NRC) determines a hop direction for the next router, not for the current router. The virtual channel allocation stage (VA) allocates output VCs to the input packets. The switch allocation stage (SA) arbitrates the crossbar switch for the flit. The switch traversal stage (ST) delivers the packet across the crossbar to the output buffer. The link traversal stage (LT) traverses the packet from the output buffer to the next router.

**2.2 Process Variation In Asynchronous Noc Design:**

As a consequence of the existence of PV in NoC design,variation in the maximum operating frequency of individual cores is to be determined in the traditional synchronous NoC.Synchronous router sends a grant message in every clockcycle. Therefore, the frequencies of all routers in synchronous design should match the lowest frequency. As a result, the saturation throughput and the network performance degrade as the impact of PV increases in fully synchronous design.The effect of PV on network performance of synchronous NoC is very systematic. On the other hand, asynchronous NoC requires deeper analysis. The asynchronous NoC router sends a grant message when it gets a request or after it finishes transmitting a flit. Consequently, each router in asynchronous NoC design can be operated with its own maximum frequency since the communication between the routers is organized by the handshaking process.

To determine the delay variation under PV conditions,asynchronous NoC routers are designed. Asynchronous router is divided into input port (IP), output port (OP), and routing control unit (RCU). The IP includes dual-to-single converter,asynchronous single rail FIFO, and single-to-dual converter.The OP is composed of C-elements and dual-rail module.A bidirectional point-to-point interconnects are used in the communication between any two routers or a router and a local resource. In addition, external lines are added to each router to exchange the information about the congestion and delay with PV (DPV) with its neighbors as described in the followingsection. The handshake protocols are the bundled-data encoding for single-rail protocol and the delay-insensitive encoding for dual-rail protocol. Handshaking signals are necessary to synchronize data transfer between processing elements (PEs)in asynchronous design. Global interconnects are distributed among the routers to transfer data and acknowledgment (ACK)signals. RCU is used to implement the routing algorithm and select the suitable OP for incoming message. The structure of asynchronous router is implemented to evaluate the delaywith/without PV.

Random variation has two primary components: 1) gate variation and 2) interconnect variation. Random variation of logic gates changes the threshold voltage and effective channel length of the transistor. Interconnect variation occurs in interconnect dimensions [width (*W*), height (*H*), space (*S*), and dielectric thickness (*T* )]. One of the major problems in NoCdesign is the considerable mismatch between two identical devices that occurs when the amount of random variation increases. PV increases the variance of delay compared with nominal values. The impact of gate delay variation on asynchronous NoC. Interconnect delay variation is important to be considered in calculating delay variation for asynchronous NoC router.

*A. Router Delay Variation:*

The threshold voltage (*V*th*)* and effective channellength (*L*gate*)* are statistically independent and follow Gaussian distribution. Negligible spatial correlation exists between *L*gate and *V*th of devices. The variation in circuit delay isconsidered using Monte Carlo (MC) simulation. In each MC iteration, the delay due to PV in asynchronous router is evaluated using the average value of delays for all MC iterations since the handshaking protocols are responsible for transferring valid data before starting the following transmission. Assuming a large NoC size, the number of ports is determined by multiplying the number of routers By the number of ports per router. The total number of ports in the network is *M*. For network of *M* ports, the average(or mean) delay determines the delay of any port. Circuitdelay for each router is determined as follows:

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*B. Interconnect Delay Variation*

Assuming that the dimension parameters are statistically independent and follow Gaussian distribution, the variation in the electrical model of interconnect (resistance, inductance,and capacitance) is determined. For data and ACK lines, the interconnect delay for each iteration $i$ , $D\text{int}-i$ is evaluatedby considering the whole path from driver to load including*RLC* model of the line and the inserted repeaters.

For$M$ iterations, the average of the evaluated interconnect delayis given by

$D\text{int} = M-1$

$i=0\ D\text{int}-i$

The total delay for asynchronous router $D$ASR is calculated as follows:

$D\text{ASR} = D\text{rout} + D\text{int}.$

The total delay under PV has a significant impact on circuit performance. From another point of view, the delayvariation is the major reason to deteriorate the performanceof different routing algorithms.

## III. STDR ALGORITHM

Deterministic routing algorithms on the contrary to the most adaptive routing algorithmsdefine the path from the source to destination irrespective of the congestion in the network. Adaptive routing algorithms outperform deterministic ones since adaptive algorithms aim to select the less congested paths to produce load balance in the network,especially under realistic traffic loads. However, taking the congestion only into consideration is not effective methodology since random PV leads to diverse delays for each router and interconnect in network topology. Thereby, the adaptive routing algorithm that ignores the DPV can select path with low congestion but with high delay which leads to reduction in the overall NoC performance. Proceeding from this point,the adaptive routing algorithm should be aware of the DPV and congestion to determine the most appropriate path..Saturation Throughtput and Delay aware algorithm(STDR) is introduced for asynchronous NoC routers . PDCR gathers information about the congestion and DPV of the adjacent neighbors to be able to make routing decision. DPV can be defined using test flit (TF) messages.

*A. Test Flit Description.*

Globally asynchronous locally synchronous technique is used by implementing asynchronous NoC design to apply the handshake protocols between each two adjacent routers,and provide a synchronous interface with each PE. The local clocks in the PEs are used to determine the timestamp (TS) to measure DPV. Local clocks in the PE are usually much faster than the communication speed.

***STDR Procedure:***

The proposed algorithm can be divided into two procedures:

**1)** Determining target node (TN) and 2) selection criterionfor the OP**.**

1) ***Determining Target Node:*** At source router, a random intermediate (IM) router is chosen between the source and the destination as an IM station during the message trip. There by,the message has two phases ($ph0$ and $ph1$*)* when it is routed from the source to the destination. At $ph0$, the message is routed from the source to the IM node. $ph1$ is used when the message is forwarded from the IM router to the destination router. This technique is used to avoid the congestion regions . In PDCR, a uniform random distribution function is used to select a random IM router between the source and destination. In addition, phase ($ph$) and IM fields are added into each message to retain the values of the message phase and the IM router identification (ID).Each router needs to declare the TN whether it is the IM or destination router. When each router forwards the message to the TN, it applies *XY* and *YX* routing algorithms to calculate the OP direction (i.e., $N = 0$). The integer value of the output direction is denoted by *Pxy* when *XY* routing algorithm is used.*Pyx* denotes the integer value of the output direction when *YX* routing algorithm is used to route the message for TN.

The default value of $ph$ field of the message is set to zero.However, $ph$ field of the message is assured from $ph0$ to $ph1$ in one of the following cases:

1) if the current router is the IM router;

2) if the curr$R$ exists in the same row of the destination router ($rx == dx$ );3) if the curr$R$ exists in the same column of the destination router ($ry == dy$);

where the coordinates of current router are $rx$ for $X$ coordinator and $ry$ for $Y$ coordinator. In addition, $dx$ is used for the $X$ coordinator of the destination node and $dy$ is used for the $Y$ coordinator of the destination node. If one of the three conditions is true, this is sufficient to make $ph$ field equal to one, and hence, the TN is assigned to the destination router ID. On the other hand, when none of the three conditions is achieved, $ph$ field equals zero and hence the TN is assigned IM field of the message.

The last two conditions are used to avoid the packet exploiting the same path more than one time during arrival trip to the destination. Exploiting the same path more than once .The source node, destination node, and IM node are chosen at *(*0, 1*)*, *(*2, 3*)*, and *(*2, 0*)*, respectively. The path is calculated from srcID to IM nodes based on DPV and congestion. The source (0, 1*)* routes the packet to *(*1, 1*)* and *(*2, 1*)* as the next hops.

Then, the packet is forwarded to the IM *(*2, 0*)*.In the second phase, the packet is routed from the IM node to desID. Based on DPV and congestion, the packet is sent from IM (2, 0) to *(*2, 1*)*.In this case, the IM node and the destination node are on the same row.

2)***Selection Criterion:***

Consequently, when the packet reach node *(*2, 1*)*, the phase is changed from $ph0$ to $ph1$ and the TN is assigned to the destination router ID *(*2, 3*)* instead of IM *(*2, 0*)*, Therefore, the last two $ph$ conditions are used to avoid such a scenario. After applying *XY* and *YX* routing algorithms, PDCR distinguishes between these two output directions (*Pxy*, *Pyx )* based on the congestion and DPV.At each router, the congestion (*Cxy)* of the neighbor router and the DPV (*xyPV)* between the curr$R$ and the neighbor router (if *XY* routing algorithm is used) are compared with the congestion (*Cyx )* of the neighbor router and the DPV (*yx PV)* between the curr$R$ and the neighbor router (if *YX* routing algorithm is used). The Data passed(diip) in the form of bits, based on the format of the packets,according to the bits are represented that source, destination and also contains payloads information. Output direction Routerxy equals the output direction Routeryx, then the propose updown

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routes to this direction.Based on the state signal, the corresponding pass to the concern router via do updown signal.

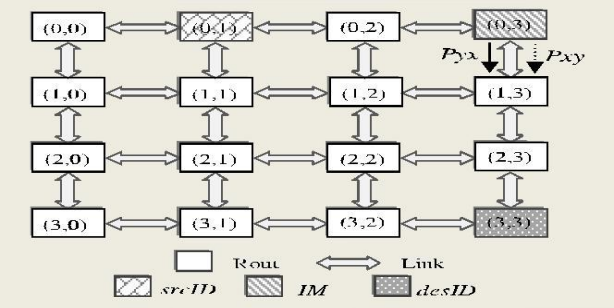


Fig:Same Direction to OP

## IV. FUZZY LOGIC

The fuzzy logic controller is composed of three main components: Fuzzification, Fuzzy Inference mechanisim and Defuzzification. Below Fig shows the components of fuzzy logic controller.First we have to fuzify the inputs or create membership values and put them into the fuzzy sets which are normalized in the range of (0,1). The Fuzzification transforms the crisp value of the input variable into the fuzzy sets. Many types of curves can be used but triangular or trapezodical shaped membership functions are the most common.The inference mechanisim applies reasoning to compute fuzzy output. Mamdani's method is the most commonly used in applications, due to its simple structure of 'min-max' operations. It consistsof a number of conditional IF THEN rules that describe the system behaviour and determine which output ranges are used. Defuzzification is the process of producing a quantifiable result and converts the fuzzy control action into a crisp value.The defuzzification interface converts the fuzzy conclusions of the inference mechanism reaches to a numeric value. Center-of-Gravity is the one of the most important method indefuzification which finds the geometrical centre. Another method for defuzzification is Mean-Of-Maxima which finds the value with the maximum membership degreeaccording to the fuzzy membership function.

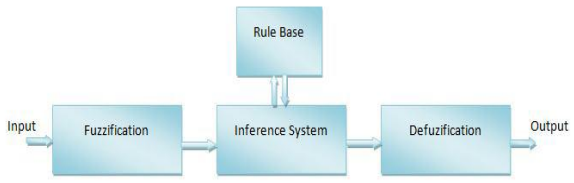


Fig :Fuzzy controller.

## IV. SIMULATION RESULTS

Average message delay and saturation throughput are the two metrics which are used to evaluate the performance of routing algorithms. The saturation throughput occurs when no additional messages can be injected successfully to the network.It can be measured at the injection rate where the average message delay reaches twice the average zero load (the lower bound on the average message delay).

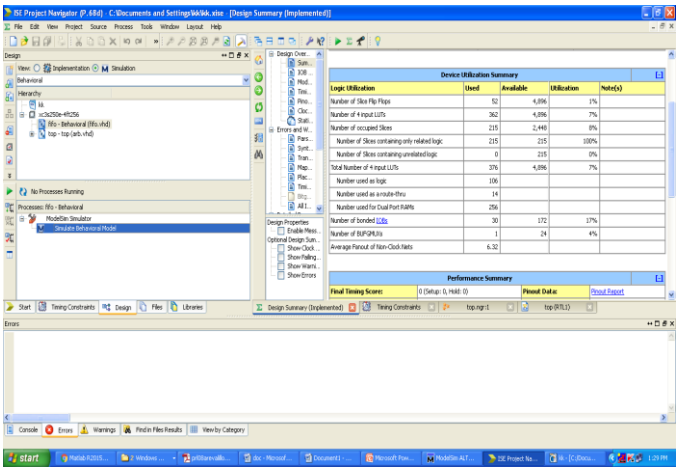

Fig: Design summary.

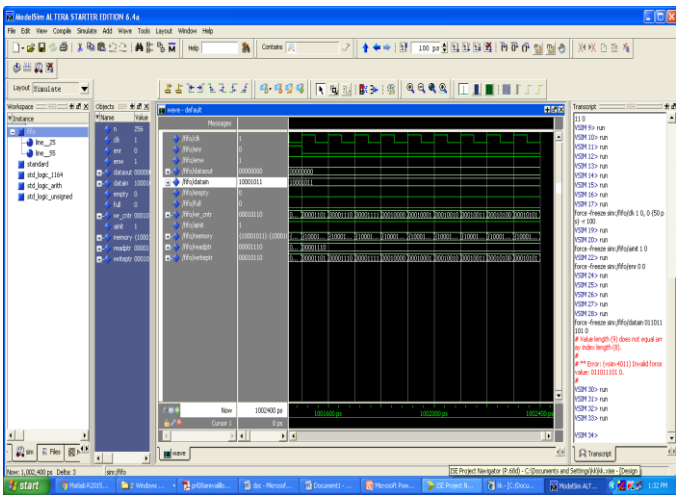

Fig: simulation result.

## V. CONCLUSION

Delay variation in logic gates and interconnect is produced as a result of PV which impacts NoC design. The delay variation is a major reason to deteriorate the performance of the routing algorithms. PV decreases the saturation throughput and increases the average message delay relative to nominal. Due to the PV, different routing algorithms can saturate at lower injection rate relative to the nominal under various traffic patterns. STDR routing algorithm is adaptive, low cost and scalable for asynchronous NoC design.It outperforms against different adaptive routing algorithms in the average delay and saturation throughput for various traffic patterns. STDR can achieve up to 12%–32% average message delay lower than that of other routing algorithms and saturation throughput by up to 11%–82% compared with other adaptive routing algorithms.

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